AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A clock extracting circuit for extracting a clock timing signal synchronous with input NRZ (Non-Return-to-Zero) type serial data from the serial data, said clock extracting circuit comprising:

oversampling means for oversampling said serial data using a reference clock signal of 2N ~~(where N is an integer of two or more)~~ times a frequency of said serial data, where N is an integer of two or more;

first timing detecting means for detecting the timing of 2N periods of said reference clock signal in a period of time in which the level of an output signal from said oversampling means remains unchanged;

second timing detecting means for detecting the timing of change in the level of the output signal from said oversampling means; and

clock timing signal outputting means for outputting ~~a~~ the clock timing signal according to the timings detected by said first timing detecting means and said second timing detecting means.

2. (Original) A clock extracting circuit as claimed in claim 1, wherein

said first timing detecting means includes:

first edge detecting means for outputting a pulse signal having a width of N periods of said reference clock signal at a point of change in the level of the output signal from said oversampling means; and

toggle means for outputting a signal inverted in polarity alternately at every N periods of said reference clock signal during a period of time from a point in time when the output signal from said first edge detecting means makes a transition from a first level to a second level lower than said first level to

a point in time when said output signal of said first edge detecting means makes a next transition from said second level to said first level; and

said second timing detecting means includes:

second edge detecting means for outputting a pulse signal having a width of one period of said reference clock signal at the point of change in the level of the output signal from said oversampling means; and

delay means for delaying the output signal from said second edge detecting means by N periods of said reference clock signal.

3. (Original) A clock extracting circuit as claimed in claim 2, wherein said toggle means outputs said second level when the output signal from said first edge detecting means is at said first level.

4. (Original) A clock extracting circuit as claimed in claim 2, wherein said clock timing signal outputting means includes logical calculation means for calculating a logical sum of output signals from said toggle means and said delay means.

5. (Previously Presented) A clock extracting circuit as claimed in claim 2, further comprising data output means for delaying the output signal from said oversampling means by (N – 1) periods of said reference clock signal and outputting the delayed signal as data corresponding to said clock timing signal.

6. (Original) A clock extracting circuit as claimed in claim 1, further comprising a phase-locked loop circuit for generating said reference clock signal as a single-phase signal.

7. (Previously Presented) A clock extracting method for extracting a clock timing signal synchronous with input NRZ (Non-Return-to-Zero) type serial data from the serial data, said clock extracting method comprising the steps of:

oversampling said serial data using a reference clock signal of 2N ~~(where N is an integer of two or more)~~ times a frequency of said serial data, where N is an integer of two or more; and

generating ~~a~~ the clock timing signal according to the timing of 2N periods of said reference clock signal, said timing being detected in a period of time in which the level of a signal generated by said oversampling remains unchanged, and timing of change in the level of the signal generated by said oversampling.